WHAT IS CLAIMED IS:

1. A communication transmission apparatus, comprising:

a first input for receiving coded bits;

a second input for receiving an interleaved version of said coded bits;

a first mapper coupled to said first input for applying a first coded bits-to-signal mapping to said coded bits to produce a first output signal;

a second mapper coupled to said second input for applying a second coded bits-to-signal mapping to the interleaved version of said coded bits to produce a second output signal, wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping; and

a communication channel interface coupled to said mappers for interfacing said output signals to a communication channel.

2. The apparatus of Claim 1, wherein said communication channel interface is a wireless communication channel interface.

3. The apparatus of Claim 1, provided as one of a wireless telephone, a laptop computer and a personal digital assistant.

4. The apparatus of Claim 1, wherein said first mapping is one of Gray mapping, 0231 mapping and 0213 mapping.

5. The apparatus of Claim 4, wherein said second mapping is another of Gray mapping, 0231 mapping and 0213 mapping.

6. The apparatus of Claim 1, wherein said first mapping is set partition mapping.

7. The apparatus of Claim 1, wherein said first mapper and said second mapper each implement one of QPSK mapping and 8PSK mapping.

8. The apparatus of Claim 1, wherein said communication channel interface includes a combiner coupled to said first and second mappers for combining said first and second output signals to produce a combined output signal for interfacing to the communication channel.

9. The apparatus of Claim 1, wherein said first mapper and said second mapper each implement one of 4-PAM mapping and 6-PAM mapping.

10. The apparatus of Claim 1, including a third mapper coupled to said first input for applying a third coded bits-to-signal mapping to said coded bits to produce said first output signal, wherein said third coded bits-to-signal mapping differs from said first coded bits-to-signal mapping, and further including a selection apparatus connected between said first input and said first and third mappers for selecting one of said first and

third mappers to apply its associated coded bits-to-signal mapping to said coded bits to produce said first output signal.

11. The apparatus of Claim 10, wherein said third coded bits-to-signal mapping is the same as said second coded bits-to-signal mapping.

12. The apparatus of Claim 11, wherein said selection apparatus includes an input for receiving information indicative of a relative frequency with which said first and second coded bits-to-signal mappings are to be applied to produce said output signals, said selection apparatus responsive to said relative frequency information for switching between said first and third mappers to implement said relative frequency.

13. The apparatus of Claim 1, including a third mapper coupled to said second input for applying a third coded bits-to-signal mapping to the interleaved version of said coded bits to produce said second output signal, wherein said third coded bits-to-signal mapping differs from said second coded bits-to-signal mapping, and further including a selection apparatus connected between said second input and said second and third mappers for selecting one of said second and third mappers to apply its associated coded bits-to-signal mapping to the interleaved version of said coded bits to produce said second output signal.

14. The apparatus of Claim 13, wherein said third coded bits-to-signal mapping is the same as said first coded bits-to-signal mapping.

15. The apparatus of Claim 14, wherein said selection apparatus includes an input for receiving information indicative of a relative frequency with which said second and first coded bits-to-signal mappings are to be applied to produce said output signal, said selection apparatus responsive to said relative frequency information for switching between said second and third mappers to implement said relative frequency.

16. A parallel concatenated trellis-coded modulation apparatus, comprising:

an input for receiving uncoded bits from a communication application;

a first coder coupled to said input for producing coded bits from said uncoded bits;

an interleaver coupled to said input for producing from said uncoded bits an interleaved version of said uncoded bits;

a second coder coupled to said interleaver for producing an interleaved version of said coded bits from the interleaved version of said uncoded bits;

a first mapper coupled to said first coder for applying a first coded bits-to-signal mapping to said coded bits to produce a first output signal; and

a second mapper coupled to said second coder for applying a second coded bits-to-signal mapping to the interleaved version of said coded bits to produce a second output

signal, wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.

17. The apparatus of Claim 16, wherein said interleaver includes first and second interleaver portions for respectively interleaving most significant bits and least significant bits of said uncoded bits, and wherein said first and second interleaver portions are different length interleaver portions.

18. The apparatus of Claim 17, wherein said first and second interleaver portions are 4096-bit interleaver portions.

19 The apparatus of Claim 16, wherein said first and second coders each implement an identical recursive systematic component code.

20. The apparatus of Claim 16, wherein said first mapping is one of Gray mapping, 0231 mapping and 0213 mapping.

21. The apparatus of Claim 20, wherein said second mapping is another of Gray mapping, 0231 mapping and 0213 mapping.

22. The apparatus of Claim 16, wherein said first mapping is set partition mapping.

23. The apparatus of Claim 16, wherein said first mapper and said second mapper each implement one of QPSK mapping and 8PSK mapping.

24. The apparatus of Claim 16, wherein said first mapper and said second mapper each implement one of 4-PAM mapping and 6-PAM mapping.

25. A communication transmission method, comprising:

receiving coded bits and an interleaved version of said coded bits;

applying a first coded bits-to-signal mapping to said coded bits to produce a first output signal;

applying a second coded bits-to-signal mapping to the interleaved version of said coded bits to produce a second output signal, wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping; and

interfacing said output signals to a communication channel.

26. The method of Claim 25, wherein said interfacing step includes interfacing said output signals to a wireless communication channel.

27. The method of Claim 25, including applying a third coded bits-to-signal mapping to said coded bits to produce said first output signal, wherein said third coded bits-to-signal mapping differs from said first coded bits-to-signal mapping, and further

including selectively applying one of said first and third coded bits-to-signal mappings to said coded bits to produce said first output signal.

28. The method of Claim 27, wherein said third coded bits-to-signal mapping is the same as said second coded bits-to-signal mapping.

29. The method of Claim 28, including receiving information indicative of a relative frequency with which said first and second coded bits-to-signal mappings are to be applied to produce said output signals, and said selectively applying step including switching between said first and third coded bits-to-signal mappings to implement said relative frequency.

30. The method of Claim 25, including applying a third coded bits-to-signal mapping to the interleaved version of said coded bits to produce said second output signal, wherein said third coded bits-to-signal mapping differs from said second coded bits-to-signal mapping, and further including selectively applying said second and third coded bits-to-signal mappings to the interleaved version of said coded bits to produce said second output signal.

31. The method of Claim 30, wherein said third coded bits-to-signal mapping is the same as said first coded bits-to-signal mapping.

32. The method of Claim 31, including receiving information indicative of a relative frequency with which said second and first coded bits-to-signal mappings are to be applied to produce said output signals, and said selectively applying step including switching between said second and third coded bits-to-signal mappings to implement said relative frequency.

33. The method of Claim 25, wherein said interfacing step includes combining said first and second output signals to produce a combined output signal for interfacing to the communication channel.

34. A method of performing parallel concatenated trellis-coded modulation, comprising:

receiving uncoded bits from a communication application;

encoding said uncoded bits to produce coded bits;

interleaving said uncoded bits to produce an interleaved version of said uncoded bits;

encoding the interleaved version of said uncoded bits to produce an interleaved version of said coded bits;

applying a first coded bits-to-signal mapping to said coded bits to produce a first output signal; and

applying a second coded bits-to-signal mapping to the interleaved version of said coded bits to produce a second output signal, wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.

35. The method of Claim 34, wherein said interleaving step includes using a first interleaving operation for interleaving most significant bits of said uncoded bits and using a second interleaving operation for interleaving least significant bits of said uncoded bits, wherein said first and second interleaving operations are different length interleaving operations.

36. The method of Claim 35, wherein said first and second interleaving operations are each 4096-bit interleaving operations.

37. The method of Claim 34, wherein said encoding steps each implement an identical recursive systematic component code.